THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

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PAT.&T.M. OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte IAN D. LEWIS and PRESTON A. HAUCK

Appeal No. 96-0335
Application 07/676,167[1]

ON BRIEF

Before THOMAS, HAIRSTON and KRASS, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 20.

The disclosed invention relates to a method and apparatus for supplying initial instructions from one computer to a second computer via a communications interface.

[1] Application for patent filed March 27, 1991.

Claims 1 and 12 are illustrative of the claimed invention, and they read as follows:

1. A computer system, comprising:

a first computer;

a second computer having stored therein a plurality of initial instructions for said first computer

communications interface means operatively connected to said first and second computers for allowing communication between said first and second computers;

transfer means for transferring said plurality of initial instructions from said second computer to said communications interface;

reset means controlled by said second computer for resetting said first computer; and

decoding means operatively associated with said first computer for addressing said communications interface when said first computer outputs an address falling within the address space of said initial instructions whereby said first computer obtains its initial instructions from said second computer through said communications interface.

12. In a computer system having first and second computers and a communications interface allowing communication between said first and second computers, a method of providing initial instructions to said first computer, comprising:

storing said initial instructions for said first computer in said second computer;

writing said initial instructions from said second computer to said communications interface; and

resetting said first computer from said second computer;

decoding the address from which said computer fetches initial instructions to cause said communications interface to be addressed when said first computer outputs an address falling within the address space of said initial instructions whereby

said first computer obtains its initial instructions from said second computer through said communications interface.

The references relied on by the examiner are:

Mathews	4,590,551	May 20, 1986
Svinicki et al. (Svinicki)	4,896,289	Jan. 23, 1990
Dayan et al. (Dayan)	5,187,792	Feb. 16, 1993 (filed May 9, 1990)

Rosenberg[2], Dictionary of Computers, Information Processing & Telecommunications, 1984, page 97.

Claims 1 through 11 stand rejected under the second paragraph of 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter that appellant regards as the invention.

Claims 1 through 20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Svinicki in view of Mathews and Rosenberg.

Claim 14 stands rejected under 35 U.S.C. § 103 as being unpatentable over Svinicki in view of Mathews, Rosenberg[3] and Dayan.

Reference is made to the briefs and the answer for the respective positions of the appellants and the examiner.

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[2] Since an excerpt from Rosenberg's computer dictionary is used in the grounds of rejection, it should have been included in the listing of the prior art of record relied upon by the examiner.

[3] If the Rosenberg excerpt is included in the grounds of rejection of independent claim 12, then it is included in the grounds of rejection of dependent claim 14.

OPINION

We have carefully considered the entire record before us, and we will reverse all of the rejections.

In the indefiniteness rejection of claims 1 through 11, the examiner indicates [Answer, page 4] that:

> As to claim 1, the structural relationship between the reset means and the decoding means is not clear. For example, if the reset means is removed from the system, can the decoding means still address the communication interface?

Turning to appellants' disclosure for an understanding of the "relationship" between the reset means and the decoding means, we find that pages 25 through 27 of the specification specifically describe the "relationship" between the reset means and the decoding means in the overall computer system that allows communication between Computer A and Computer B via the communications interface 18. For example, the second full paragraph on page 26 of the specification states that:

> The reset signal of Computer B is controlled by Computer A. At the time at which Computer A causes the reset signal of Computer B to become inactive, the address decoding circuits of Computer B are configured such that when Computer B fetches instructions from the memory locations from which the initial instructions are fetched, Computer B reads from the FIFO buffer in the communications interface.

As clearly set forth in the disclosure, the reset means and the decoding means are both necessary means for the proper operation of the disclosed and claimed computer system. If the reset means

is removed from the computer system, then Computer B can not be reset, and the decoding means in Computer B can not fetch the initial instructions from the communications interface. Thus, we agree with appellants' argument [Brief, page 11] that "[s]ince the structural relationship between the reset means and the decoding means is clearly illustrated in the specification, the claim cannot be considered indefinite." The indefiniteness rejection of claims 1 through 11 is reversed.

Turning to the obviousness rejection of claims 1 through 20, the examiner indicates [Answer, pages 4 and 5] that Svinicki teaches the invention substantially as claimed by including in his system an expansion system interface connection to several personal computers in Figures 1 and 2. According to the examiner, the system further includes a first processor 20, a second computer 12, 14, 16 or 18, communications interface 10, transfer means 37, and reset means (i.e., the pre-boot controlled by one of the second computers for resetting the first processor. The examiner acknowledges [Answer, page 6] that "Svinicki did not specifically show the decoding means for addressing the communication interface when a first computer outputs an address space of the initial instructions to obtain the initial instructions from the second computer through the interface means as claimed." The secondary reference to Mathews is cited by the examiner because it discloses "a network processor [NSP]

interfaced between a host (second computer in the claim) and a line processor [LSP] (first computer in the claim; e.g. see fig. 16) in which request/result messages, such as Initialize Adapter and Clear LSP...were sent over to the line processor [LSP] by the host processor through the network processor." The examiner is of the opinion [Answer, pages 6 and 7] that for the purpose of transferring the initial instruction messages from the second computer (i.e., the host) to the first computer (LSP), Mathews must have included a decoding means for addressing the interface network (NSP) because "without knowing the address of the interface network, the interface communication between first and second computers can not be achieved." The examiner then concludes that it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to "use Matthews [sic, Mathews] in Svinicki for addressing the interface means and for obtaining the initial instructions as claimed because the use of Matthews [sic, Mathews] could provide access of the initialization program of Svinicki personal computers to one another, and because Svinicki suggested the need for obtaining initial instructions from one computer by another." The Rosenberg Computer Dictionary excerpt is relied on by the examiner because it shows the "well known meaning of the term: "CLEAR" used as for the purpose of initialization (i.e. to a prescribed state)."

We note that the examiner has labeled the electronic typesetter 20 or 22 in Svinicki as a processor. For purposes of claim analysis and comparison to the applied prior art, we assume the examiner is referring to the typesetter as a computer. In any event, we find that Svinicki is concerned with the relationship between one of the computers 12, 14, 16 or 18 and the interface 10. A careful review of Svinicki reveals that the typesetter is only tangential to the relationship between the computers 12, 14, 16 or 18 and the typesetter. In other words, Svinicki is primarily concerned with the efficient movement of data from one of the noted computers through the interface to the typesetter, and is not concerned with using one of the computers 12, 14, 16 or 18 to directly control the typesetter 10. As a result thereof, the initialization system and reset condition discussed in column 6, lines 10 through 49 are not for use by the typesetter.

We agree with appellants' argument [Brief, page 10] that Mathews does not describe the presence of a decoder in his system "or indicate how such non-existent decoder could possibly be used in the system of Svinicki to produce the claimed invention. More importantly, we agree with appellants' argument that "[e]ven if Mathews did disclose a decoder of some type, it is not at all clear how it could be used in the Svinicki et al. system." We are, therefore, of the opinion that appellants correctly

concluded [Brief, page 10] that the system disclosed by Svinicki has no need of a decoder. As a result thereof, the obviousness rejection of claims 1 through 20 is reversed.

The obviousness rejection of claim 14 is reversed because the additional reference to Dayan was only cited [Answer, page 9] to show "a RAM which included write protected address space to prevent changes to BIOs during system operation (e.g. see col. 8 lines 20-40)."

DECISION

The decision of the examiner rejecting claims 1 through 11 under the second paragraph of 35 U.S.C. § 112, and claims 1 through 20 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS
Administrative Patent Judge)
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KENNETH W. HAIRSTON) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
)
ERROL A. KRASS) INTERFERENCES
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